Claims 5 and 6 and renumber the original Claims 5 to 21 as Claims 7 to 23. The dependence of renumbered Claim 6 is on renumbered Claim 5. The dependence of renumbered Claim 15 is on renumbered Claim 14. The dependence of renumbered Claim 16 is on renumbered Claim 14. The dependence of renumbered Claim 17 is on renumbered Claim 14. The dependence of renumbered Claim 18 is on renumbered Claim 14. The dependence of renumbered Claim 19 is on renumbered Claim 14. The dependence of renumbered Claim 20 is on renumbered Claim 14.

As noted above, Applicant elected to pursue group 1, claims 1-20 in Paper No. 7 filed 9/24/02, without traverse.

REMARKS

Pending in this Application are Claims 1-20.

Rejections Under 35 U.S.C. 102(b)

Claims 14 and 17

Claims 14 and 17 stand rejected under 35 U.S.C. 102(e) as being anticipated by being anticipated by U.S. Patent No. 6,350,631 to Kobayashi et al. ("Kobayashi"). In paragraph 3 of page 2 of the Office Action, the Examiner states: "Kobayashi, et al. disclose (see specifically figure 1) a surface-mount semiconductor device package comprising: a planar ceramic substrate 32 having a first surface (e.g., top surface) and an opposing second surface (e.g., bottom surface); a semiconductor device 14 disposed on the substrate first surface; conductive pads 21-24 disposed on the substrate second surface; conductive leads 15-16 coupling the semiconductor device to the conductive pads; an epoxy resin 25, having low dielectric constant, encapsulating the semiconductor device 14 and the substrate first surface."

Claim 14

As for Claim 14, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 14, as amended, provides:

14. A surface mount semiconductor device package comprising:

a planar ceramic substrate having a first surface and an opposing second surface;

a semiconductor device disposed on the substrate first surface;

conductive pads disposed on the substrate second surface;

conductive leads coupling the semiconductor device to the conductive pads;

a low dielectric constant encapsulant material encapsulating the semiconductor device and substrate first surface;

said conductive leads with lengths such that the series inductance of the device package is minimized; and

said encapsulant material having a composition such that the parasitic capacitance of the device package is minimized.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract). Kobayashi is not directed toward semiconductor devices with high frequency uses.

In order to achieve Kobayashi's mentioned objective, an electronic device of the Kobayashi invention is obtained by mounting plural sets of electronic components on a ceramic substrate and sealing the electronic components with thermosetting resin by transfer molding. The electronic device is provided with metallic thin film integrated into at least one selected from an upper surface and a lower surface of the ceramic substrate at its peripheral portion (Column 4 lines 17-25).

More specifically, Figure 1 of Kobayashi shows a sectional side view of a three-terminal leadless small surface mount transistor provided with three electrodes including a collector electrode, a base electrode, and an emitter electrode (Column 8, lines 36-39). The thickness of the ceramic substrate was set to be 0.15 to 0.20 mm. The via holes have a diameter of approximately 0.10 mm and are provided in predetermined places of the ceramic substrate. Inside the via holes, a conductive paste is injected to form conductors. The conductors formed inside these via holes serve as conductive relay members for electrically connecting the upper electrodes and the lower electrodes (Column 8, lines 45-54). The transistor shown in Figure 1, the first metal wire, and the second metal wire are coated with thermosetting resin (for instance, epoxy resin using bisphenol A or cresolnovolac glycidyl ether resin as a base) *for transfer molding* that generally had been used conventionally. A coating method is described in a third embodiment of the Kobayashi invention. The coating thickness of the resin for transfer molding is set to be 0.35 to 0.39 mm (Column 8, lines 66-67 and Column 9, lines 1-8).

It is instructive to note that Kobayashi does not specifically require the use of a low dielectric constant encapsulant material. That is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

For a prior-art reference to anticipate under 35 U.S.C. Section 102, every element of the claimed invention must be identically shown in a single reference. These elements must be arranged as in the claimed under review. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567-68 (Fed. Cir. 1990). As such, Kobayashi cannot anticipate Claim 14 or any of its respective dependent claims.

Claim 17

As for Claim 17, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 17 provides:

17. A surface-mount semiconductor device package according to claim 14 wherein the encapsulant material comprises epoxy resin.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract).

In order to achieve Kobayashi's mentioned objective, an electronic device of the Kobayashi invention is obtained by mounting plural sets of electronic components on a ceramic substrate and sealing the electronic components with thermosetting resin by transfer molding. The electronic device is provided with metallic thin film integrated into at least one selected from an upper surface and a lower surface of the ceramic substrate at its peripheral portion (Column 4 lines 17-25).

More specifically, Figure 1 of Kobayashi shows a sectional side view of a three-terminal leadless small surface mount transistor provided with three electrodes including a collector electrode, a base electrode, and an emitter electrode (Column 8, lines 36-39). The thickness of the ceramic substrate was set to be 0.15 to 0.20 mm. The via holes have a diameter of approximately 0.10 mm and are provided in predetermined places of the ceramic substrate. Inside the via holes, a conductive paste is injected to form conductors. The conductors formed inside these via holes serve as conductive relay members for electrically connecting the upper electrodes and the lower electrodes (Column 8, lines 45-54). The transistor shown in Figure 1, the first metal wire, and the second metal wire are coated with thermosetting resin (for instance, epoxy resin using bisphenol A or cresolnovolac glycidyl ether resin as a base) *for transfer molding* that generally had been used conventionally. A coating method is described in a third embodiment of the Kobayashi invention. The coating thickness of the resin for transfer molding is set to be 0.35 to 0.39 mm (Column 8, lines 66-67 and Column 9, lines 1-8).

It is instructive to note that Kobayashi does not specifically require the use of a low dielectric constant encapsulant material. That is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

For a prior-art reference to anticipate under 35 U.S.C. Section 102, every element of the claimed invention must be identically shown in a single reference. These elements must be arranged as in the claimed under review. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567-68 (Fed. Cir. 1990). Since Kobayashi cannot anticipate Claim 14, it cannot anticipate Claim 17, one of its respective dependent claims.

Rejections Under 35 U.S.C. 103(a)

Claims 1, 5-7 and 10-11 and 18

Claims 1, 5-7 and 10-11 and 18 stand as rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of U.S. Patent No. 6,117,797 to Hembree ("Hembree"). In paragraph 5 of page 3 of the Office Action, the Examiner states: "Regarding claims 1, 5-7, 10-11 and 18, Kobayashi et al. disclose all the limitations of the claimed invention as detailed above except for the epoxy resin being Dexter FP4451 epoxy resin.

Dexter FP4451 epoxy resin, however, is conventionally used in the art as an encapsulant material and available from the DEXTER ELECTRONIC MATERIALS DIVISION OF DEXTER CORPORATION, etc. as disclosed by Hembree (Col. 6, lines 60+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the well known Dexter FP4451 epoxy resin, as taught by Hembree, to Kobayashi et al.'s device package to encapsulate the semiconductor device and the substrate first surface, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. As a result, the encapsulant,

which is made of Dexter FP4451 epoxy resin, would inherently has thermal expansion properties substantially similar to the thermal expansion properties of the substrate, which is made of ceramic."

Applicant will first point out why the teaching of **each** of the cited references is different from the claimed invention, and then demonstrate why the **combination** of the cited references still fails to render the claimed invention obvious.

Claim 1

As for Claim 1, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 1, as amended, provides:

> 1. A surface-mount semiconductor device package comprising:
>
> a substrate having at least one planar surface;
>
> a semiconductor device disposed on the planar surface of the substrate;
>
> an encapsulant surrounding the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate;
>
> a plurality of conductive leads lengths such that the series inductance of the device package is minimized; and
>
> said encapsulant material having a composition such that the parasitic capacitance of the device package is minimized.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract).

In order to achieve Kobayashi's mentioned objective, an electronic device of the Kobayashi invention is obtained by mounting plural sets of electronic components on a ceramic substrate and sealing the electronic components with thermosetting resin by transfer molding. The electronic device is provided with metallic thin film integrated into at least one selected from an upper surface and a lower surface of the ceramic substrate at its peripheral portion (Column 4 lines 17-25).

More specifically, Figure 1 of Kobayashi shows a sectional side view of a three-terminal leadless small surface mount transistor provided with three electrodes including a collector electrode, a base electrode, and an emitter electrode (Column 8, lines 36-39). The thickness of the ceramic substrate was set to be 0.15 to 0.20 mm. The via holes have a diameter of approximately 0.10 mm and are provided in predetermined places of the ceramic substrate. Inside the via holes, a conductive paste is injected to form conductors. The conductors formed inside these via holes serve as conductive relay members for electrically connecting the upper electrodes and the lower electrodes (Column 8, lines 45-54). The transistor shown in Figure 1, the first metal wire, and the second metal wire are coated with thermosetting resin (for instance, epoxy resin using bisphenol A or cresolnovolac glycidyl ether resin as a base) *for transfer molding* that generally had been used conventionally. A coating method is described in a third embodiment of the Kobayashi invention. The coating thickness of the resin for transfer molding is set to be 0.35 to 0.39 mm (Column 8, lines 66-67 and Column 9, lines 1-8).

It is instructive to note that Kobayashi does not disclose nor specifically require the use of a low dielectric constant encapsulant material. This is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

Applicant further respectfully responds that Hembree relates to the manufacture of Chip On Board devices with heat sinks for high power dissipation (Column 1, lines 6-10). Hembree teaches a means of keeping glob top material off the semiconductor device so as to permit the attachment of a heat sink or other heat dispersal apparatus to the semiconductor device. Hembree does not teach

covering the semiconductor device with an encapsulant with thermal properties substantially similar to the thermal expansion of the substrate.

More specifically, in one aspect of Hembree, a thermally conducting interface material of filled gel elastomer material or a silicone elastomeric material or other elastomeric material is applied to the die surface to which the heat sink is to be bonded. In accordance with the Hembree invention, a method for fabricating a Chip On Board semiconductor device requiring enhanced heat dissipation is applicable to direct attachment of semiconductor devices, such as dynamic memory semiconductor die, to substrates, such as circuit boards and the like, and to the formation of modules incorporating a substrate, such as a circuit board. In one aspect of the Hembree invention, an elastomer is used to cover a portion of a semiconductor die prior to glob top application of the die to the circuit board. The elastomer is removed, e.g. by peeling, from the die surface and includes any glob top material which has inadvertently been applied to the elastomer. Thus, the portion of the semiconductor die remains free of contaminants. Since a portion of the semiconductor die is free of contaminants, providing a good adhesion surface, a heat sink may be attached to such portion of the semiconductor die. The Hembree method is applicable to both wire-bonded dies and flip-chip die bonding to circuit boards. The elastomer used in Hembree may be a highly thermally conductive elastomer to enhance the heat transfer from the semiconductor die to the surrounding environment. An example of a highly thermally conductive elastomer is a metal-filled elastomer or an elastomer filled with a highly thermally conductive material like metal (Column 2, lines 29-56).

Also shown in Figure 1 of Hembree, a glob top material applied to encapsulate and seal the semiconductor die, wires, and surrounding portions of the substrate. According to Hembree, the glob top material may be any suitable glob top material, an encapsulant type material, etc. (Column 4, lines 4-6 and 11-12) Hembree notes that the glob top material is typically a thermally resistive polymer such as commercially available epoxy or urethane. The glob top material is typically applied as a curable liquid through a small nozzle, not shown, to extend to the layer of gel elastomer. (Column 5, lines 26-33). Application of the glob top material is followed by a curing step, such as by temperature elevation. The glob top material is cured to provide a hard, impenetrable sealing surface. (Column 5, lines 39-42) The glob top materials may be the same or different materials.

According to Hembree, glob top materials useful for this application include HYSOL™ FP4451 high purity, liquid-damming, encapsulant compatible material or HYSOL™ FP4450 high purity, low stress liquid encapsulant material, available from the DEXTER ELECTRONIC MATERIALS DIVISION OF DEXTER CORPORATION, etc. (Column 6, lines 56-63).

In essence, the focus of the Hembree invention is a method for preventing misplaced encapsulant material from adhering to a surface of a semiconductor die, as seen in independent Claims 1, 15, 28, 41, 54, 65, 69 and 80 of Hembree.

In contrast to both Kobayashi and Hembree, the present invention discloses and claims an encapsulant *surrounding* the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate. Contrary to what is claimed here, namely, the use of a *surrounding* encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrateIn contrast to both Kobayashi and Hembree, the present invention discloses and claims an encapsulant *surrounding* the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate. Contrary to what is claimed here, namely, the use of a *surrounding* encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate, Kobayashi does not teach the use of any particular encapsulant. *See*, the Title, the Abstract, and the Specification.

Also, contrary to what is claimed here, namely, the covering of the semiconductor device by said encapsulant material, Hembree teaches the use of a heat sink over, or covering, the semiconductor device, not an encapsulant as in the present invention. Claim 1 of the present invention teaches the use of the encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate over and on the sides of the semiconductor device (See Paragraph 0021, Claim 1 and Figure 1).

Claim 5

As for Claim 5, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 5 provides:

5. A surface-mount semiconductor device package according to claim 1 further comprising a plurality of conductive pads disposed on a surface of the substrate and electrically bonded to the semiconductor device.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claim 1 are equally applicable here and, to conserve resources, are incorporated by reference.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract).

It is instructive to note that Kobayashi does not disclose nor specifically require the use of a low dielectric constant encapsulant material. This is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

Applicant further respectfully responds that Hembree relates to the manufacture of Chip On Board devices with heat sinks for high power dissipation (Column 1, lines 6-10). Hembree teaches a means of keeping glob top material off the semiconductor device so as to permit the attachment of a heat sink or other heat dispersal apparatus to the semiconductor device. Hembree does not teach covering the semiconductor device with an encapsulant with thermal properties substantially similar to the thermal expansion of the substrate.

In contrast to both Kobayashi and Hembree, the present invention discloses and claims an encapsulant *surrounding* the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate.

Contrary to what is claimed here, namely, the use of a *surrounding* encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate, further comprising a plurality of conductive pads disposed on a surface of the substrate and electrically bonded to the semiconductor device, Kobayashi does not teach the use of any particular encapsulant. *See*, the Title, the Abstract, and the Specification.

Also, contrary to what is claimed here, namely, the covering of the semiconductor device by said encapsulant material, Hembree teaches the use of a heat sink over, or covering, the semiconductor device, not an encapsulant as in the present invention.

Claim 5 of the present invention teaches the use of the encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate over and on the sides of the semiconductor device, with a plurality of conductive pads disposed on the surface of the substrate and electrically bonded to the semiconductor device (See Paragraphs 0021, 0022, 0023, Claims 1 and 5 and Figure 1).

Claim 6

As for Claim 6, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 6 provides:

> 6. A surface-mount semiconductor device package according to claim 5 further comprising conductive leads for electrically coupling the conductive pads to the semiconductor device.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claim 1 are equally applicable here and, to conserve resources, are incorporated by reference.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as

to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract).

It is instructive to note that Kobayashi does not disclose nor specifically require the use of a low dielectric constant encapsulant material. This is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

Applicant further respectfully responds that Hembree relates to the manufacture of Chip On Board devices with heat sinks for high power dissipation (Column 1, lines 6-10). Hembree teaches a means of keeping glob top material off the semiconductor device so as to permit the attachment of a heat sink or other heat dispersal apparatus to the semiconductor device. Hembree does not teach covering the semiconductor device with an encapsulant with thermal properties substantially similar to the thermal expansion of the substrate.

In contrast to both Kobayashi and Hembree, the present invention discloses and claims an encapsulant *surrounding* the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate. Contrary to what is claimed here, namely, the use of a *surrounding* encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate, further comprising conductive leads for electrically coupling the conductive pads to the semiconductor device, Kobayashi does not teach the use of any particular encapsulant. *See*, the Title, the Abstract, and the Specification.

Also, contrary to what is claimed here, namely, the covering of the semiconductor device by said encapsulant material, Hembree teaches the use of a heat sink over, or covering, the semiconductor device, not an encapsulant as in the present invention.

Claim 6 of the present invention teaches the use of the encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate over and on the sides of the

semiconductor device, with conductive leads for electrically coupling the conductive pads to the semiconductor device. (See Paragraphs 0021, 0022, 0023, Claims 1 and 6 and Figure 1).

Claim 7

As for Claims 7, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 7 provides:

> 7. A surface-mount semiconductor device package according to claim 1 wherein the substrate comprises ceramic material.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claim 1 are equally applicable here and, to conserve resources, are incorporated by reference.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract).

It is instructive to note that Kobayashi does not disclose nor specifically require the use of a low dielectric constant encapsulant material. This is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

Applicant further respectfully responds that Hembree relates to the manufacture of Chip On Board devices with heat sinks for high power dissipation (Column 1, lines 6-10). Hembree teaches a means of keeping glob top material off the semiconductor device so as to permit the attachment of a heat sink or other heat dispersal apparatus to the semiconductor device. Hembree does not teach

covering the semiconductor device with an encapsulant with thermal properties substantially similar to the thermal expansion of the substrate.

In contrast to both Kobayashi and Hembree, the present invention discloses and claims an encapsulant *surrounding* the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate. Contrary to what is claimed here, namely, the use of a *surrounding* encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate, wherein the substrate comprises ceramic material, Kobayashi does not teach the use of any particular encapsulant. *See*, the Title, the Abstract, and the Specification.

Also, contrary to what is claimed here, namely, the covering of the semiconductor device by said encapsulant material, Hembree teaches the use of a heat sink over, or covering, the semiconductor device, not an encapsulant as in the present invention.

Claim 7 of the present invention teaches the use of the encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate over and on the sides of the semiconductor device, with a substrate comprised of ceramic material. (See Paragraphs 0021, 0022, 0023, Claims 1 and 7 and Figure 1).

Claim 10

As for Claims 10, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 10 provides:

> 10. A surface-mount semiconductor device package according to claim 1 wherein the encapsulant material comprises epoxy resin.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claim 1 are equally applicable here and, to conserve resources, are incorporated by reference.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for

manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract).

It is instructive to note that Kobayashi does not disclose nor specifically require the use of a low dielectric constant encapsulant material. This is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

Applicant further respectfully responds that Hembree relates to the manufacture of Chip On Board devices with heat sinks for high power dissipation (Column 1, lines 6-10). Hembree teaches a means of keeping glob top material off the semiconductor device so as to permit the attachment of a heat sink or other heat dispersal apparatus to the semiconductor device. Hembree does not teach covering the semiconductor device with an encapsulant with thermal properties substantially similar to the thermal expansion of the substrate.

In contrast to both Kobayashi and Hembree, the present invention discloses and claims an encapsulant *surrounding* the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate. Contrary to what is claimed here, namely, the use of a *surrounding* encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate, wherein the encapsulant material comprises epoxy resin, Kobayashi does not teach the use of any particular encapsulant. *See*, the Title, the Abstract, and the Specification.

Also, contrary to what is claimed here, namely, the covering of the semiconductor device by said encapsulant material, Hembree teaches the use of a heat sink over, or covering, the semiconductor device, not an encapsulant as in the present invention. Claim 10 of the present invention teaches the use of the encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate over and on the sides of the semiconductor device, where the

encapsulant material comprises epoxy resin. (See Paragraphs 0021, 0022, 0023, Claims 1 and 10 and Figure 1).

Claim 11

As for Claims 11, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 11 provides:

> 11. A surface-mount semiconductor device package according to claim 1 wherein the encapsulant material comprises Dexter FP4451 epoxy resin.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claim 1 are equally applicable here and, to conserve resources, are incorporated by reference.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract).

It is instructive to note that Kobayashi does not disclose nor specifically require the use of a low dielectric constant encapsulant material. This is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

Applicant further respectfully responds that Hembree relates to the manufacture of Chip On Board devices with heat sinks for high power dissipation (Column 1, lines 6-10). Hembree teaches a means of keeping glob top material off the semiconductor device so as to permit the attachment of a heat sink or other heat dispersal apparatus to the semiconductor device. Hembree does not teach

covering the semiconductor device with an encapsulant with thermal properties substantially similar to the thermal expansion of the substrate.

In contrast to both Kobayashi and Hembree, the present invention discloses and claims an encapsulant *surrounding* the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate. Contrary to what is claimed here, namely, the use of a *surrounding* encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate, wherein the encapsulant material comprises Dexter FP4451 epoxy resin, Kobayashi does not teach the use of any particular encapsulant. *See*, the Title, the Abstract, and the Specification.

Also, contrary to what is claimed here, namely, the covering of the semiconductor device by said encapsulant material, Hembree teaches the use of a heat sink over, or covering, the semiconductor device, not an encapsulant as in the present invention. Claim 11 of the present invention teaches the use of the encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate over and on the sides of the semiconductor device, wherein the encapsulant material comprises Dexter FP4451 epoxy resin. (See Paragraphs 0021, 0022, 0023, Claims 1 and 11 and Figure 1).

Claim 18

As for Claim 18, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 18 provides:

> 18. A surface-mount semiconductor device package according to claim 14 wherein the encapsulant material comprises Dexter FP4451 epoxy resin.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claim 1 are equally applicable here and, to conserve resources, are incorporated by reference.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for

manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract).

It is instructive to note that Kobayashi does not disclose nor specifically require the use of a low dielectric constant encapsulant material. This is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

Applicant further respectfully responds that Hembree relates to the manufacture of Chip On Board devices with heat sinks for high power dissipation (Column 1, lines 6-10). Hembree teaches a means of keeping glob top material off the semiconductor device so as to permit the attachment of a heat sink or other heat dispersal apparatus to the semiconductor device. Hembree does not teach covering the semiconductor device with an encapsulant with thermal properties substantially similar to the thermal expansion of the substrate.

In contrast to both Kobayashi and Hembree, the present invention discloses and claims an encapsulant *surrounding* the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate. Contrary to what is claimed here, namely, the use of a *surrounding* encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate, Kobayashi does not teach the use of any particular encapsulant. *See*, the Title, the Abstract, and the Specification.

Also, contrary to what is claimed here, namely, the covering of the semiconductor device by said encapsulant material, Hembree teaches the use of a heat sink over, or covering, the semiconductor device, not an encapsulant as in the present invention. Claim 18 of the present invention, which is dependent on Claim 14, teaches the use of a low dielectric constant encapsulant material encapsulating the semiconductor and substrate of the first surface comprising Dexter FP4451 epoxy resin. (See Paragraphs 0021, 0022, 0023, Claims 14 and 18 and Figure 1).

With respect to Claim 18, Applicant further demonstrates below why the **combination** of the cited references still fails to render the claimed invention obvious.

Combination of References

The **combination** of the cited references fails to render the claimed invention in Claims 1, 5-7 and 10-11 and 18 obvious. Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate. Since neither invention of Kobayashi nor Hembree are optimized for high frequency use, there is no suggestion or incentive in either reference to combine the references.

Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references still falls short of rendering obvious the claimed invention.

In discussing a rejection under 35 U.S.C. 103, the Court, in *In re Wesslau*, 147 U.S.P.Q. 391, 393 (C.C.P.A. 1965) held that:

> It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of its as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art.

The Examiner may not use Applicant's claims as a blueprint to pick and choose from one of the references only so much of it as will support the Examiner's position and to exclude other parts necessary to the full appreciation of what that reference fairly suggests to one of ordinary skill in the art. This type of piecemeal reconstruction of the references in light of Applicant's disclosure is not a permissible basis for holding the invention obvious. *In re Kamm and Young*, 172 U.S.P.Q. 298, 301-302 (C.C.P.A. 1972).

The Federal Circuit has repeatedly held that hindsight must be avoided in combining reference structures. *Panduit Corp. v. Dennison Manufacturing Co.*, 227 U.S.P.Q. 337, 343 (Fed. Cir. 1985); *In re Find*, 5 U.S.P.Q.2d 1596, 1599-1560 (Fed. Cir. 1988). Thus, it is error to reconstruct a patentee's claimed invention from the prior art by using the patentee's claims as a blueprint. Prior art references must be read as a whole and consideration must be given where the references diverge and teach away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 U.S.PQ. 303, 311-13 (Fed. Cir. 1983). A claim cannot properly be used as a blueprint for abstracting individual teachings from references. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 227 U.S.P.Q. 657, 667 (Fed. Cir. 1985).

Claims 2-4

Claims 2-4 stand as rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of U.S. Patent No. 6,117,797 to Hembree ("Hembree"). In paragraph 5 of page 4 of the Office Action, the Examiner states: "Regarding claims 2-4, since the materials made of the substrate and the encapsulant of the proposed device package of Kobayashi et al. and Hembree and that of the claimed invention are similar, the proposed package would inherently have the thermal resistance as being claimed (e.g., being less than approximately 25 degrees Centigrade per Watt)."

Applicant will first point out why the teaching of **each** of the cited references is different from the claimed invention, and then demonstrate why the **combination** of the cited references still fails to render the claimed invention obvious.

Claim 2

As for Claim 2, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 2 provides:

> 2. A surface-mount semiconductor device package according to claim 1 wherein the package thermal resistance is less than about 200 degrees Centigrade per Watt.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract).

In order to achieve the mentioned objective, an electronic device of the Kobayashi invention is obtained by mounting plural sets of electronic components on a ceramic substrate and sealing the electronic components with thermosetting resin by transfer molding. The electronic device is provided with metallic thin film integrated into at least one selected from an upper surface and a lower surface of the ceramic substrate at its peripheral portion (Column 4 lines 17-25).

More specifically, Figure 1 of Kobayashi shows a sectional side view of a three-terminal leadless small surface mount transistor provided with three electrodes including a collector electrode, a base electrode, and an emitter electrode (Column 8, lines 36-39). The thickness of the ceramic substrate was set to be 0.15 to 0.20 mm. The via holes have a diameter of approximately 0.10 mm and are provided in predetermined places of the ceramic substrate. Inside the via holes, a conductive paste is injected to form conductors. The conductors formed inside these via holes serve as conductive relay members for electrically connecting the upper electrodes and the lower electrodes (Column 8, lines 45-54). The transistor shown in Figure 1, the first metal wire, and the second metal wire are coated with thermosetting resin (for instance, epoxy resin using bisphenol A or cresolnovolac glycidyl ether resin as a base) *for transfer molding* that generally had been used conventionally. A coating method is described in a third embodiment of the Kobayashi invention. The coating thickness of the resin for transfer molding is set to be 0.35 to 0.39 mm (Column 8, lines 66-67 and Column 9, lines 1-8).

It is instructive to note that Kobayashi does not disclose nor specifically require the use of a low dielectric constant encapsulant material. This is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which

occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

Applicant further respectfully responds that Hembree relates to the manufacture of Chip On Board devices with heat sinks for high power dissipation (Column 1, lines 6-10). Hembree teaches a means of keeping glob top material off the semiconductor device so as to permit the attachment of a heat sink or other heat dispersal apparatus to the semiconductor device. Hembree does not teach covering the semiconductor device with an encapsulant with thermal properties substantially similar to the thermal expansion of the substrate.

More specifically, in one aspect of Hembree, a thermally conducting interface material of filled gel elastomer material or a silicone elastomeric material or other elastomeric material is applied to the die surface to which the heat sink is to be bonded. In accordance with the Hembree invention, a method for fabricating a Chip On Board semiconductor device requiring enhanced heat dissipation is applicable to direct attachment of semiconductor devices, such as dynamic memory semiconductor die, to substrates, such as circuit boards and the like, and to the formation of modules incorporating a substrate, such as a circuit board. In one aspect of the Hembree invention, an elastomer is used to cover a portion of a semiconductor die prior to glob top application of the die to the circuit board. The elastomer is removed, e.g. by peeling, from the die surface and includes any glob top material which has inadvertently been applied to the elastomer. Thus, the portion of the semiconductor die remains free of contaminants. Since a portion of the semiconductor die is free of contaminants, providing a good adhesion surface, a heat sink may be attached to such portion of the semiconductor die. The Hembree method is applicable to both wire-bonded dies and flip-chip die bonding to circuit boards. The elastomer used in Hembree may be a highly thermally conductive elastomer to enhance the heat transfer from the semiconductor die to the surrounding environment. An example of a highly thermally conductive elastomer is a metal-filled elastomer or an elastomer filled with a highly thermally conductive material like metal (Column 2, lines 29-56).

Also shown in Figure 1 of Hembree, a glob top material applied to encapsulate and seal the semiconductor die, wires, and surrounding portions of the substrate. According to Hembree, the glob top material may be any suitable glob top material, an encapsulant type material, etc. (Column

4, lines 4-6 and 11-12) Hembree notes that the glob top material is typically a thermally resistive polymer such as commercially available epoxy or urethane. The glob top material is typically applied as a curable liquid through a small nozzle, not shown, to extend to the layer of gel elastomer. (Column 5, lines 26-33). Application of the glob top material is followed by a curing step, such as by temperature elevation. The glob top material is cured to provide a hard, impenetrable sealing surface. (Column 5, lines 39-42) The glob top materials may be the same or different materials. According to Hembree, glob top materials useful for this application include HYSOL™ FP4451 high purity, liquid-damming, encapsulant compatible material or HYSOL™ FP4450 high purity, low stress liquid encapsulant material, available from the DEXTER ELECTRONIC MATERIALS DIVISION OF DEXTER CORPORATION, etc. (Column 6, lines 56-63). The focus of the Hembree invention is a method for preventing misplaced encapsulant material from adhering to a surface of a semiconductor die, as seen in independent Claims 1, 15, 28, 41, 54, 65, 69 and 80 of Hembree.

In contrast to both Kobayashi and Hembree, the present invention discloses and claims an encapsulant *surrounding* the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate. Contrary to what is claimed here, namely, the use of a *surrounding* encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate, wherein the package thermal resistance is less than about 200 degrees Centigrade per Watt, Kobayashi does not teach the use of any particular encapsulant. *See*, the Title, the Abstract, and the Specification.

Also, contrary to what is claimed here, namely, the covering of the semiconductor device by said encapsulant material, Hembree teaches the use of a heat sink over, or covering, the semiconductor device, not an encapsulant as in the present invention. Claim 1 of the present invention teaches the use of the encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate over and on the sides of the semiconductor device (See Paragraph 0021, Claim 1 and Figure 1).

Claim 3

As for Claim 3, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 3 provides:

> 3. A surface-mount semiconductor device package according to claim 1 wherein the package thermal resistance is less than about 50 degrees Centigrade per Watt.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claim 2 are equally applicable here and, to conserve resources, are incorporated by reference.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract).

In order to achieve the mentioned objective, an electronic device of the Kobayashi invention is obtained by mounting plural sets of electronic components on a ceramic substrate and sealing the electronic components with thermosetting resin by transfer molding. The electronic device is provided with metallic thin film integrated into at least one selected from an upper surface and a lower surface of the ceramic substrate at its peripheral portion (Column 4 lines 17-25).

It is instructive to note that Kobayashi does not disclose nor specifically require the use of a low dielectric constant encapsulant material. This is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which

occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

Applicant further respectfully responds that Hembree relates to the manufacture of Chip On Board devices with heat sinks for high power dissipation (Column 1, lines 6-10). Hembree teaches a means of keeping glob top material off the semiconductor device so as to permit the attachment of a heat sink or other heat dispersal apparatus to the semiconductor device. Hembree does not teach covering the semiconductor device with an encapsulant with thermal properties substantially similar to the thermal expansion of the substrate.

In contrast to both Kobayashi and Hembree, the present invention discloses and claims an encapsulant *surrounding* the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate. Contrary to what is claimed here, namely, the use of a *surrounding* encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate, wherein the package thermal resistance is less than about 50 degrees Centigrade per Watt, Kobayashi does not teach the use of any particular encapsulant. *See*, the Title, the Abstract, and the Specification.

Also, contrary to what is claimed here, namely, the covering of the semiconductor device by said encapsulant material, Hembree teaches the use of a heat sink over, or covering, the semiconductor device, not an encapsulant as in the present invention. Claim 1 of the present invention teaches the use of the encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate over and on the sides of the semiconductor device (See Paragraph 0021, Claim 1 and Figure 1).

Claim 4

As for Claim 4, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 4 provides:

4. A surface-mount semiconductor device package according to claim 1 wherein the package thermal resistance is less than approximately 25 degrees Centigrade per Watt.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claim 2 are equally applicable here and, to conserve resources, are incorporated by reference.

Applicant respectfully responds that Kobayashi and Figure 1 of Kobayashi teach an electronic device with a substantially planar upper surface, and the method and apparatus for manufacturing same. The object of the invention of Kobayashi is to prevent the occurrence of cracks or breakage in the ceramic substrate by buffering the pressure applied to the ceramic substrate so as to prevent a distortion force from being caused even when the ceramic substrate is sandwiched and compressed between upper and lower molds (See Abstract).

In order to achieve the mentioned objective, an electronic device of the Kobayashi invention is obtained by mounting plural sets of electronic components on a ceramic substrate and sealing the electronic components with thermosetting resin by transfer molding. The electronic device is provided with metallic thin film integrated into at least one selected from an upper surface and a lower surface of the ceramic substrate at its peripheral portion (Column 4 lines 17-25).

It is instructive to note that Kobayashi does not disclose nor specifically require the use of a low dielectric constant encapsulant material. This is because the invention of Kobayashi is not directed toward high frequency uses. The present invention advantageously discloses and claims a method and apparatus that overcomes difficulties in the generation of parasitic capacitance which occurs at high frequencies by using an encapsulation material over the semiconductor device with a low dielectric constant.

Applicant further respectfully responds that Hembree relates to the manufacture of Chip On Board devices with heat sinks for high power dissipation (Column 1, lines 6-10). Hembree teaches a means of keeping glob top material off the semiconductor device so as to permit the attachment of a heat sink or other heat dispersal apparatus to the semiconductor device. Hembree does not teach

covering the semiconductor device with an encapsulant with thermal properties substantially similar to the thermal expansion of the substrate.

In contrast to both Kobayashi and Hembree, the present invention discloses and claims an encapsulant *surrounding* the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate. Contrary to what is claimed here, namely, the use of a *surrounding* encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate, wherein the package thermal resistance is less than approximately 25 degrees Centigrade per Watt, Kobayashi does not teach the use of any particular encapsulant. *See*, the Title, the Abstract, and the Specification.

Also, contrary to what is claimed here, namely, the covering of the semiconductor device by said encapsulant material, Hembree teaches the use of a heat sink over, or covering, the semiconductor device, not an encapsulant as in the present invention. Claim 1 of the present invention teaches the use of the encapsulant with thermal expansion properties similar to the thermal expansion properties of the substrate over and on the sides of the semiconductor device (See Paragraph 0021, Claim 1 and Figure 1).

Combination of References

The **combination** of the cited references fails to render the claimed invention in Claims 2-4 obvious. Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate. Since neither invention of Kobayashi nor Hembree are optimized for high frequency use, there is no suggestion or incentive in either reference to combine the references.

Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references still falls short of rendering obvious the claimed invention.

In discussing a rejection under 35 U.S.C. 103, the Court, in *In re Wesslau*, 147 U.S.P.Q. 391, 393 (C.C.P.A. 1965) held that:

> It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of its as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art.

The Examiner may not use Applicant's claims as a blueprint to pick and choose from one of the references only so much of it as will support the Examiner's position and to exclude other parts necessary to the full appreciation of what that reference fairly suggests to one of ordinary skill in the art. This type of piecemeal reconstruction of the references in light of Applicant's disclosure is not a permissible basis for holding the invention obvious. *In re Kamm and Young*, 172 U.S.P.Q. 298, 301-302 (C.C.PA. 1972).

The Federal Circuit has repeatedly held that hindsight must be avoided in combining reference structures. *Panduit Corp. v. Dennison Manufacturing Co.*, 227 U.S.P.Q. 337, 343 (Fed. Cir. 1985); *In re Find*, 5 U.S.P.Q.2d 1596, 1599-1560 (Fed. Cir. 1988). Thus, it is error to reconstruct a patentee's claimed invention from the prior art by using the patentee's claims as a blueprint. Prior art references must be read as a whole and consideration must be given where the references diverge and teach away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 U.S.PQ. 303, 311-13 (Fed. Cir. 1983). A claim cannot properly be used as a blueprint for abstracting individual teachings from references. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 227 U.S.P.Q. 657, 667 (Fed. Cir. 1985).

Claims 8-9 and 15-16

Claims 8-9 and 15-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Hembree and further in view of U.S. Patent No. 5,296,074 to Graham et al. ("Graham"). In paragraph 6 of page 4 of the Office Action, the states: "Regarding claims 8-9 and 15-16, the proposed device package of Kobayashi et al. and Hembree discloses all the limitations of the claimed invention as detailed above except for the substrate comprising alumina (as recited in claims 8 and 15) or berylia (as recited in claims 9 and 16).

Alumina and berylia, however, are two well-known materials in the art for making a ceramic substrate, as disclosed by Graham et al (col. 5, lines 35+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use alumina or berylia for the device package of Kobayashi et al. and Hembree, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416."

Applicant will first point out why the teaching of **each** of the cited references is different from the claimed invention, and then demonstrate why the **combination** of the cited references still fails to render the claimed invention obvious.

Claim 8

As for Claim 8, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 8 provides:

> 8. A surface-mount semiconductor device package according to claim 1 wherein the substrate comprises alumina.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claims 1 and 2 are equally applicable here and, to conserve resources, are incorporated by reference.

Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular

encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate. With respect to Graham, the invention of Graham is directed to a method for rapidly bonding a small electronic component to a mating surface of a high surface energy substrate comprising the sequential steps of:

(1) Forming a continuous filament of non-olefinic, substantially amorphous, solvent-free thermoplastic polymer, at least one diameter of which is substantially equal to or greater than a lateral dimension of a mating surface of the small electronic component, the polymer being further characterized in that

T_g is at least 30°C,

T_b is below -30°C,

S_w is less than 1.0% wt., and

Extractable ionics are less than10 ppm by wt.;

(2) Cutting the filament to form an adhesive pad having both lateral dimensions substantially equal to or greater than a corresponding lateral dimensions of the mating surface of the small electronic component and having a thickness of 25-125 micrometers;

(3) Simultaneously preheating the mating surfaces of both the substrate and the small electronic component so that a temperature of the surfaces exceeds the T_g of the amorphous adhesive;

(4) Positioning the adhesive pad upon the heated substrate surface with an application of slight pressure to effect heat transfer from the substrate to the adhesive pad, thus softening the adhesive without incurring adhesive flow;

(5) Positioning the heated small electronic component upon the heated adhesive pad;

(6) Laminating the small electronic component to the substrate by applying a higher pressure to the small electronic component to reduce the thickness of the adhesive pad by 0.5 to 5% and releasing the pressure on the small electronic component within 2 seconds; and

(7) Cooling the laminated component assembly. (Column 1, lines 60-68 and Column 2, lines 1-30)

Graham notes that ceramic substrates are generally ceramic oxides of which Al_2O_3 and SiO_2 predominate. As noted therein, previously fired patterned substrates such as those laid down from screen-printed conductor, resistor and dielectric thick films and from green tapes may also be used. Other ceramic substrate materials cited in Graham include BeO, AIN and metal core substrates such as porcelain enameled steel. All of the substrates cited in Graham are characterized by high energy surfaces which are wetted by the non-olefinic polymeric materials used in the Graham invention. (Column 5, lines 35-46).

The disclosure and claims of Graham are predicated on a method for rapidly bonding a small electronic component having a mating surface smaller than about one square inch selected from the class consisting of capacitor, transistor, resistor, diode and integrated circuit chip to a substrate employing an adhesive pad between the electronic component and the substrate (Column 10, lines 4-10).

Graham does not discuss the thermal expansion properties of the encapsulant material covering the semiconductor device, nor does it discuss the thermal expansion properties of the substrate. A number of different substrate materials are mentioned in Graham, none of which are cited particularly for their thermal expansion characteristics. Graham focuses on the use of an adhesive pad between the electronic component and the substrate so as to improve the manufacturing process. None of the inventions of Kobayashi, Hembree or Graham are optimized for high frequency use, nor do they address issues related to the thermal expansion coefficients of the substrate and the semiconductor device. There is no suggestion or incentive in any of the reference to combine them.

Claim 9

As for Claim 9, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 9 provides:

9. A surface-mount semiconductor device package according to claim 1 wherein the substrate comprises beryllia.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claims 1 and 2 and the Graham invention with respect to Claim 8 are equally applicable here and, to conserve resources, are incorporated by reference.

Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate.

The disclosure and claims of Graham are predicated on a method for rapidly bonding a small electronic component having a mating surface smaller than about one square inch selected from the class consisting of capacitor, transistor, resistor, diode and integrated circuit chip to a substrate employing an adhesive pad between the electronic component and the substrate (Column 10, lines 4-10).

Graham does not discuss the thermal expansion properties of the encapsulant material covering the semiconductor device, nor does it discuss the thermal expansion properties of the substrate. A number of different substrate materials are mentioned in Graham, none of which are cited particularly for their thermal expansion characteristics. Graham focuses on the use of an adhesive pad between the electronic component and the substrate so as to improve the manufacturing process. None of the inventions of Kobayashi, Hembree or Graham are optimized for high frequency use, nor do they address issues related to the thermal expansion coefficients of the substrate and the semiconductor device. There is no suggestion or incentive in any of the references to combine them.

Claim 15

As for Claim 15, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 15 provides:

> 15. A surface-mount semiconductor device package according to claim 14 wherein the substrate comprises alumina.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claims 1 and 2 and the Graham invention with respect to Claim 8 are equally applicable here and, to conserve resources, are incorporated by reference.

Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate.

The disclosure and claims of Graham are predicated on a method for rapidly bonding a small electronic component having a mating surface smaller than about one square inch selected from the class consisting of capacitor, transistor, resistor, diode and integrated circuit chip to a substrate employing an adhesive pad between the electronic component and the substrate (Column 10, lines 4-10).

Graham does not discuss the thermal expansion properties of the encapsulant material covering the semiconductor device, nor does it discuss the thermal expansion properties of the substrate. A number of different substrate materials are mentioned in Graham, none of which are cited particularly for their thermal expansion characteristics. Graham focuses on the use of an adhesive pad between the electronic component and the substrate so as to improve the manufacturing

process. None of the inventions of Kobayashi, Hembree or Graham are optimized for high frequency use, nor do they address issues related to the thermal expansion coefficients of the substrate and the semiconductor device. There is no suggestion or incentive in any of the references to combine them.

Claim 16

As for Claim 16, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 16 provides:

> 16. A surface-mount semiconductor device package according to claim 14 wherein the substrate comprises beryllia.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claims 1 and 2 and the Graham invention with respect to Claim 8 are equally applicable here and, to conserve resources, are incorporated by reference.

Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate. The disclosure and claims of Graham are predicated on a method for rapidly bonding a small electronic component having a mating surface smaller than about one square inch selected from the class consisting of capacitor, transistor, resistor, diode and integrated circuit chip to a substrate employing an adhesive pad between the electronic component and the substrate (Column 10, lines 4-10).

Graham does not discuss the thermal expansion properties of the encapsulant material covering the semiconductor device, nor does it discuss the thermal expansion properties of the substrate. A number of different substrate materials are mentioned in Graham, none of which are

cited particularly for their thermal expansion characteristics. Graham focuses on the use of an adhesive pad between the electronic component and the substrate so as to improve the manufacturing process. None of the inventions of Kobayashi, Hembree or Graham are optimized for high frequency use, nor do they address issues related to the thermal expansion coefficients of the substrate and the semiconductor device. There is no suggestion or incentive in any of the references to combine them.

Combination of References

The **combination** of the cited references fails to render the claimed invention in Claims 8-9 and 15-16 obvious. Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate. Since neither invention of Kobayashi nor Hembree are optimized for high frequency use, there is no suggestion or incentive in either reference to combine the references. Graham focuses on the use of an adhesive pad between the electronic component and the substrate so as to improve the manufacturing process. Graham does not discuss the thermal expansion properties of the encapsulant material covering the semiconductor device, nor does it discuss the thermal expansion properties of the substrate. A number of different substrate materials are mentioned in Graham, none of which are cited particularly for their thermal expansion characteristics. None of the inventions of Kobayashi, Hembree or Graham are optimized for high frequency use, nor do they address issues related to the thermal expansion coefficients of the substrate and the semiconductor device. There is no suggestion or incentive in any of the reference to combine them.

Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references still falls short of rendering obvious the claimed invention.

In discussing a rejection under 35 U.S.C. 103, the Court, in *In re Wesslau*, 147 U.S.P.Q. 391, 393 (C.C.P.A. 1965) held that:

> It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of its as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art.

The Examiner may not use Applicant's claims as a blueprint to pick and choose from one of the references only so much of it as will support the Examiner's position and to exclude other parts necessary to the full appreciation of what that reference fairly suggests to one of ordinary skill in the art. This type of piecemeal reconstruction of the references in light of Applicant's disclosure is not a permissible basis for holding the invention obvious. *In re Kamm and Young*, 172 U.S.P.Q. 298, 301-302 (C.C.PA. 1972).

The Federal Circuit has repeatedly held that hindsight must be avoided in combining reference structures. *Panduit Corp. v. Dennison Manufacturing Co.*, 227 U.S.P.Q. 337, 343 (Fed. Cir. 1985); *In re Find*, 5 U.S.P.Q.2d 1596, 1599-1560 (Fed. Cir. 1988). Thus, it is error to reconstruct a patentee's claimed invention from the prior art by using the patentee's claims as a blueprint. Prior art references must be read as a whole and consideration must be given where the references diverge and teach away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 U.S.PQ. 303, 311-13 (Fed. Cir. 1983). A claim cannot properly be used as a blueprint for abstracting individual teachings from references. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 227 U.S.P.Q. 657, 667 (Fed. Cir. 1985).

Claims 12-13 and 19-20

Claims 12-13 and 19-20 stand as rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al. (6,350,631) in view of Hembree (6,117,797) and further in view of Hashizume (5,946,556). In paragraph 7 of page 5 of the Office Action, the Examiner states: "Regarding claims 12-13 and 19-20, the proposed device package of Kobayashi et al. and Hembree discloses all the

limitations of the claimed invention as detailed above except for the semiconductor device being operable at frequencies within a range of about 2-20 GHZ (claims 12 and 19) or 10-12 GHZ (claims 13 and 20).

The device that is able to operate at frequencies within a range of about 2-20 GHZ or 10-12 GHZ, however, is conventional in the art, as disclosed by Hashizume (Col. 1, lines 15+), and it is well known within the skills of an artisan to choose the most suitable semiconductor device, depending on the application in hand."

Applicant will first point out why the teaching of **each** of the cited references is different from the claimed invention, and then demonstrate why the **combination** of the cited references still fails to render the claimed invention obvious.

Claim 12

As for Claim 12, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 12 provides:

> 12. A surface-mount semiconductor device package according to claim 1 wherein the semiconductor device is operable at frequencies within a range of about 2-10 GHz.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claims 1 and 2 are equally applicable here and, to conserve resources, are incorporated by reference.

Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate.

The invention of Hashizume relates to a fabrication method of a plastic-packaged semiconductor device and more particularly, to a fabrication method of a semiconductor device equipped with a semiconductor element chip such as an Integrated Circuit (IC) chip and a plastic package for protecting the chip, in which the package has a cavity near bonding pads or connecting terminals of the chip. (Column 1, lines 6-13).

Hashizume states that it has been known that the electrical characteristics of the microwave semiconductor element tend to degrade due to the parasitic capacitance caused by a dielectric (e.g., synthetic resin or ionic impurity) existing near the bonding pads or connecting terminals of the element or IC chip. Therefore, the microwave semiconductor element chip needs to be packaged in such a way that a hollow cavity is formed in the vicinity of the bonding pads inside the plastic package, thereby removing selectively the packaging plastic material from the vicinity of the bonding pads. To cope with this need, a prior art plastic package structure as shown in Figures 1 and 2 are disclosed. (Column 1, lines 19-30)

Hashizume discloses a fabrication method of a semiconductor device for use at high frequencies. In the first step, a wax with a property of being solid at room temperature is melted due to heat and the melted wax is coated to cover connecting terminals or electrodes of a semiconductor element chip, thereby forming a wax layer at a location where a cavity is formed.

In the second step, the wax layer and the chip are covered with a liquid-like thermosetting packaging resin produced by dissolution in a solvent.

In the third step, the packaging resin covering the wax layer and the chip is cured to form a plastic package and at the same time, the wax layer is melted to penetrate into the plastic package due to application of heat at a first temperature, thereby forming the cavity inside the plastic package by elimination of the wax layer at the location where the wax layer has been formed.

In the fourth step, a residue of the wax layer left in the cavity is vaporized due to application of heat at a second temperature, thereby removing the residue of the wax layer from the cavity. (Column 5, lines 46-65).

Hashizume focuses on the fabrication of a high frequency semiconductor device such that a hollow cavity is formed between the device and the covering plastic package. The present invention

accomplishes high frequency operation without the use of a hollow cavity between the semiconductor device and the epoxy resin packaging. Further, the use of a plastic package in Hashizume results in very inconsistent performance of the semiconductor as compared with the use of the epoxy of the present invention. Meanwhile, neither of the inventions of Kobayashi or Hembree are optimized for high frequency use, nor do they address issues related to the thermal expansion coefficients of the substrate and the semiconductor device. There is no suggestion or incentive in any of the references to combine them.

Claim 13

As for Claim 13, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 13 provides:

> 13. A surface-mount semiconductor device package according to claim 1 wherein the semiconductor device is operable at frequencies within a range of about 10-12 GHz.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claims 1 and 2 and Hashizume invention with respect to Claim 12 are equally applicable here and, to conserve resources, are incorporated by reference.

Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate.

The invention of Hashizume relates to a fabrication method of a plastic-packaged semiconductor device and more particularly, to a fabrication method of a semiconductor device

equipped with a semiconductor element chip such as an Integrated Circuit (IC) chip and a plastic package for protecting the chip, in which the package has a cavity near bonding pads or connecting terminals of the chip. (Column 1, lines 6-13)

Hashizume focuses on the fabrication of a high frequency semiconductor device such that a hollow cavity is formed between the device and the covering plastic package. The present invention accomplishes high frequency operation without the use of a hollow cavity between the semiconductor device and the epoxy resin packaging. Meanwhile, neither of the inventions of Kobayashi or Hembree are optimized for high frequency use, nor do they address issues related to the thermal expansion coefficients of the substrate and the semiconductor device. There is no suggestion or incentive in any of the references to combine them..

Claim 19

As for Claim 19, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 19 provides:

> 19. A surface-mount semiconductor device package according to claim 14 wherein the semiconductor device is operable at frequencies within a range of about 2-10 GHz.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claims 1 and 2 and the Hashizume invention of Claim 12 are equally applicable here and, to conserve resources, are incorporated by reference. Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate.

The invention of Hashizume relates to a fabrication method of a plastic-packaged semiconductor device and more particularly, to a fabrication method of a semiconductor device equipped with a semiconductor element chip such as an Integrated Circuit (IC) chip and a plastic package for protecting the chip, in which the package has a cavity near bonding pads or connecting terminals of the chip. (Column 1, lines 6-13)

Hashizume focuses on the fabrication of a high frequency semiconductor device such that a hollow cavity is formed between the device and the covering plastic package. The present invention accomplishes high frequency operation without the use of a hollow cavity between the semiconductor device and the epoxy resin packaging. Meanwhile, neither of the inventions of Kobayashi or Hembree are optimized for high frequency use, nor do they address issues related to the thermal expansion coefficients of the substrate and the semiconductor device. There is no suggestion or incentive in any of the references to combine them.

Claim 20

As for Claim 20, Applicant respectively traverses the Examiner's rejection and reasoning. Claim 20 provides:

> 20. A surface-mount semiconductor device package according to claim 14 wherein the semiconductor device is operable at frequencies within a range of about 10-12 GHz.

The general discussion of the Kobayashi and Hembree inventions above with respect to Claims 1 and 2 and the Hashizume invention of Claim 12 are equally applicable here and, to conserve resources, are incorporated by reference. Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off

the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate.

The invention of Hashizume relates to a fabrication method of a plastic-packaged semiconductor device and more particularly, to a fabrication method of a semiconductor device equipped with a semiconductor element chip such as an Integrated Circuit (IC) chip and a plastic package for protecting the chip, in which the package has a cavity near bonding pads or connecting terminals of the chip. (Column 1, lines 6-13)

Hashizume focuses on the fabrication of a high frequency semiconductor device such that a hollow cavity is formed between the device and the covering plastic package. The present invention accomplishes high frequency operation without the use of a hollow cavity between the semiconductor device and the epoxy resin packaging. Meanwhile, neither of the inventions of Kobayashi or Hembree are optimized for high frequency use, nor do they address issues related to the thermal expansion coefficients of the substrate and the semiconductor device. There is no suggestion or incentive in any of the references to combine them.

Combination of References

The **combination** of the cited references fails to render the claimed invention in Claims 12-13 and 10-12 obvious. Kobayashi is not optimized for high frequency use and thus does not teach or suggest the use of a low dielectric constant encapsulant material; Hembree does not disclose the use of a particular encapsulant material *covering* the semiconductor device; and, in fact, Hembree teaches a method of keeping glob top or other encapsulant material off the surface of the semiconductor device. In Hembree, conventional epoxy resins are used to couple the edges of the semiconductor die to the substrate. Since neither invention of Kobayashi nor Hembree are optimized for high frequency use, there is no suggestion or incentive in either reference to combine the references. Hashizume focuses on the fabrication of a high frequency semiconductor device such that a hollow cavity is formed between the device and the covering plastic package. The present invention accomplishes high frequency operation without the use of a hollow cavity between the semiconductor device and the epoxy resin packaging. Meanwhile, neither of the inventions of

Kobayashi or Hembree are optimized for high frequency use, nor do they address issues related to the thermal expansion coefficients of the substrate and the semiconductor device. There is no suggestion or incentive in any of the reference to combine them.

Thus, without using hindsight of selective picking and choosing, Applicant respectfully submits that the combination of the references still falls short of rendering obvious the claimed invention.

In discussing a rejection under 35 U.S.C. 103, the Court, in *In re Wesslau*, 147 U.S.P.Q. 391, 393 (C.C.P.A. 1965) held that:

> It is impermissible within the framework of Section 103 to pick and choose from any one reference only so much of its as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art.

What the Examiner cannot do is using Applicant's claims as a blueprint to pick and choose from one of the references only so much of it as will support the Examiner's position and to exclude other parts necessary to the full appreciation of what that reference fairly suggests to one of ordinary skill in the art. This type of piecemeal reconstruction of the references in light of Applicant's disclosure is not a permissible basis for holding the invention obvious. *In re Kamm and Young*, 172 U.S.P.Q. 298, 301-302 (C.C.PA. 1972).

The Federal Circuit has repeatedly held that hindsight must be avoided in combining reference structures. *Panduit Corp. v. Dennison Manufacturing Co.*, 227 U.S.P.Q. 337, 343 (Fed. Cir. 1985); *In re Find*, 5 U.S.P.Q.2d 1596, 1599-1560 (Fed. Cir. 1988). Thus, it is error to reconstruct a patentee's claimed invention from the prior art by using the patentee's claims as a blueprint. Prior art references must be read as a whole and consideration must be given where the references diverge and teach away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 U.S.PQ. 303, 311-13 (Fed. Cir. 1983). A claim cannot properly be used as a blueprint for abstracting individual teachings from references. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 227 U.S.P.Q. 657, 667 (Fed. Cir. 1985).

Other Cited Art

The Examiner cited U.S. Pat. No. 6,392,294 to Yamaguchi ("Yamaguchi"); U.S. Pat. No. 6,121,637 to Isokawa et al ("Isokawa"); and U.S. Pat. No. 6,383,835 to Hata et al. ("Hata") for showing the surface-mount semiconductor device package.

Yamaguchi is directed toward a semiconductor device is provided which includes an insulating substrate, a conductive terminal supported by the substrate, a semiconductor chip mounted on the substrate, and a protection coating for enclosing the chip. The protection coating is integrally formed with an anchoring portion. The substrate is formed with an engaging portion for engagement with the anchoring portion of the coating. (Abstract). In contrast, the present invention is directed toward a surface mount semiconductor device package with a low dielectric constant encapsulant material encapsulating a semiconductor device, the semiconductor device having conductive leads with lengths such that the series inductance of the device package is minimized and the encapsulant material having a composition such that the parasitic capacitance of the device package is minimized. The disclosure of Yamaguchi does not address encapsulant material nor the length of conductive leads, which are key characteristics of the present invention.

Isokawa is directed toward a chip-type light emitting device in which first and second terminal electrodes are formed on both ends of an insulating substrate with a light emitting device chip being mounted on the surface side, the LED chip is directly formed on the insulating substrate, and at least a portion of the insulating substrate on which the LED chip is mounted is formed by a whitish material. Alternatively, in a lamp-type semiconductor light emitting device in which the LED chip is mounted on the top of a lead, and is covered with a dome-shaped package, or in a chip-type semiconductor light emitting device, a bonding material used for bonding the LED chip is made of a whitish material. Therefore, it becomes possible to reflect light that proceeds toward the back surface side of the LED chip efficiently, and consequently to increase the necessary luminosity even if the light-emitting efficiency inside the LED chip remains the same. (Abstract). In contrast, the present invention is directed toward a surface mount semiconductor device package with a low dielectric constant encapsulant material encapsulating a semiconductor device, the semiconductor

device having conductive leads with lengths such that the series inductance of the device package is minimized and the encapsulant material having a composition such that the parasitic capacitance of the device package is minimized. The disclosure of Isokawa does not address encapsulant material nor the length of conductive leads, which are key characteristics of the present invention. In fact, the key characteristic of the encapulant of Isokawa is it's ability to transmit light through it, as the semiconductor device of Isokawa is a light emitting diode.

Hata is directed toward an IC package having a substrate having recesses formed on the side wall thereof, an insulating film for covering an opening of each recess on the side of a principal surface of the substrate, and an IC chip mounted on a mount surface side of the film on the substrate, wherein a conductive portion formed on each recess is used as an external connection terminal for the IC chip. (Abstract). In contrast, the present invention is directed toward a surface mount semiconductor device package with a low dielectric constant encapsulant material encapsulating a semiconductor device, the semiconductor device having conductive leads with lengths such that the series inductance of the device package is minimized and the encapsulant material having a composition such that the parasitic capacitance of the device package is minimized. The disclosure of Isokawa does not address encapsulant material nor the length of conductive leads, which are key characteristics of the present invention.

PCT Cited Art

Included with this filing are documents cited by the European Patent Office on February 13, 2003. Each of these references are also distinguishable from the present invention.

In the Abstract of Eiichi, Japanese Application 01295864 ("Eiichi"), a method of increasing the adhesive properties of the encapsulant to the substrate is described. While the advantages of matching thermal expansion coefficients between the encapsulant and the substrate are described, several fundamental elements claimed in the present invention are not addressed in Eiichi. Eiichi does not describe any of the claims of the present invention relating to a plurality of conductive leads lengths such that the series inductance of the device package is minimized, said

encapsulant material having a composition such that the parasitic capacitance of the device package is minimized.

In the Abstract of Masaki, Japanese Application 04090909 ("Masaki"), a method of preventing a solder joint crack in an circuit board is described. In Masaki, the advantages of using a protective coating with a particular thermal coefficient is described. However, several fundamental elements claimed in the present invention are not addressed in Masaki. Masaki does not describe any of the claims of the present invention relating to a plurality of conductive leads lengths such that the series inductance of the device package is minimized, said encapsulant material of the present invention having a composition such that the parasitic capacitance of the device package is minimized.

In the Abstract of Masahide, Japanese Application 60267645 ("Masahide"), a method of interposing a resin with a higher bonding strength between a varnish and leads is described. However, several fundamental elements claimed in the present invention are not addressed by Masahide. Masahide does not describe any of the claims of the present relating to a plurality of conductive leads lengths such that the series inductance of the device package is minimized; said encapsulant material having a composition such that the parasitic capacitance of the device package is minimized.

In U.S. Pat. No. 5,771,157 to Zak ("Zak"), claims are made to a circuit board assembly process which steps of creating gold and nickel layers on the copper preparatory to the aluminum wire to copper pad bonding steps are eliminated. Zak does not address nor claim several fundamental elements claimed in the present invention. Fundamentally, Zak does not claim a plurality of conductive leads lengths such that the series inductance of the device package is minimized; said encapsulant material having a composition such that the parasitic capacitance of the device package is minimized.

In U.S. Pat. No. 5,313,365 to Pennisi, et al., ("Pennisi"), claims are made to the composition of the resin used as glob top encapsulant, particularly an organosilicon polymer, comprising substantially of alternating polycyclic hydrocarbon residues and cyclic polysiloxane residues linked through carbon-silicon bonds. Pennisi does not address nor claim several fundamental elements

claimed in the present invention. Fundamentally, Pennisi does not claim a plurality of conductive leads lengths such that the series inductance of the device package is minimized; said encapsulant material having a composition such that the parasitic capacitance of the device package is minimized.

In European Patent Application 93203416.8 to Orem ("Orem"), a low thermal resistance flip chip is disclosed. Orem claims a low cost flip chip structure that is operable to shunt heat away from the integrated circuit using a backplate/heat sink on a pedestal, a structure not relevant to, nor claimed by, the present invention. Orem does not address nor claim several fundamental elements claimed in the present invention. Fundamentally, Orem does not claim a plurality of conductive leads lengths such that the series inductance of the device package is minimized; said encapsulant material having a composition such that the parasitic capacitance of the device package is minimized.

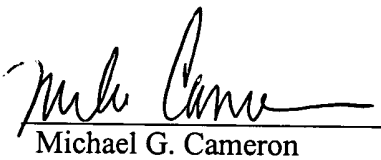
Conclusion

Applicants respectfully submit that Claims 1-20, now pending, are in condition for allowance. A Notice of Allowance is therefore requested.

If the Examiner has any other matters which pertain to this Application, the Examiner is encouraged to contact the undersigned to resolve these matters by Examiner's Amendment where possible.

Favorable consideration of the pending claims is respectfully requested.

Respectfully Submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 1, and 5-21 have been amended as follows:

WE CLAIM:

1. A surface-mount semiconductor device package comprising:

a substrate having at least one planar surface;

a semiconductor device disposed on the planar surface of the substrate; [and]

an encapsulant surrounding the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate[.] ;

a plurality of conductive leads with lengths such that the series inductance of the device package is minimized; and

said encapsulant material having a composition such that the parasitic capacitance of the device package is minimized.

5. [3] A surface-mount semiconductor device package according to claim 1 further comprising a plurality of conductive pads disposed on a surface of the substrate and electrically bonded to the semiconductor device.

6. [4] A surface-mount semiconductor device package according to claim 5 further comprising conductive leads for electrically coupling the conductive pads to the semiconductor device.

7. [5] A surface-mount semiconductor device package according to claim 1 wherein the substrate comprises ceramic material.

8. [6] A surface-mount semiconductor device package according to claim 1 wherein the substrate comprises alumina.

9. [7] A surface-mount semiconductor device package according to claim 1 wherein the substrate comprises beryllia.

10. [8] A surface-mount semiconductor device package according to claim 1 wherein the encapsulant material comprises epoxy resin.

11. [9] A surface-mount semiconductor device package according to claim 1 wherein the encapsulant material comprises Dexter FP4451 epoxy resin.

12. [10] A surface-mount semiconductor device package according to claim 1 wherein the semiconductor device is operable at frequencies within a range of about 2-10 GHz.

13. [11] A surface-mount semiconductor device package according to claim 1 wherein the semiconductor device is operable at frequencies within a range of about 10-12 GHz.

14. [12] A surface mount semiconductor device package comprising:

a planar ceramic substrate having a first surface and an opposing second surface;

a semiconductor device disposed on the substrate first surface;

conductive pads disposed on the substrate second surface;

conductive leads coupling the semiconductor device to the conductive pads; [and]

a low dielectric constant encapsulant material encapsulating the semiconductor device and substrate first surface[.] ;

said conductive leads with lengths such that the series inductance of the device package is minimized; and

said encapsulant material having a composition such that the parasitic capacitance of the device package is minimized.

15. [13] A surface-mount semiconductor device package according to claim 14 [12] wherein the substrate comprises alumina.

16. [14] A surface-mount semiconductor device package according to claim 14 [12] wherein the substrate comprises beryllia.

17. [15] A surface-mount semiconductor device package according to claim 14 wherein the encapsulant material comprises epoxy resin.

18. [16] A surface-mount semiconductor device package according to claim 14 wherein the encapsulant material comprises Dexter FP4451 epoxy resin.

19. [17] A surface-mount semiconductor device package according to claim 14 wherein the semiconductor device is operable at frequencies within a range of about 2-10 GHz.

20. [18] A surface-mount semiconductor device package according to claim 14 wherein the semiconductor device is operable at frequencies within a range of about 10-12 GHz.